U.S.S.N. 10,813,784

Specification Amendments

Please replace paragraph 003 with the following rewritten paragraph:

003 As device characteristic dimensions shrink, however, the prior art practice of forming tungsten plugs in lower metallization layers creates several problems. For example, the cost and complexity of processing increases, requiring increasingly complex processing including tungsten deposition, tungsten dry etchback, and/or CMP planarization processes to avoid respectively, for example, voids in tungsten plugs, tungsten particle contamination, and the formation of tungsten metal stringers. In addition, the electrical performance properties of tungsten, including electrical resistance are less than adequate for characteristic device dimensions less than about 0.25 microns. Moreover, the high temperature deposition processes currently required for tungsten as well as overlying

conventional copper metallization leads to undesirable defects in previously deposited metallization layers.

Please replace paragraph 0013 with the following rewritten paragraph:

0013 Referring to Figures 1A-1E, in an exemplary embodiment of the method of the present invention, cross sectional side view portions of a multi-level integrated circuit ~~is~~ are shown at stages in an exemplary manufacturing process. Referring to Figure 1A, is shown a semiconductor substrate 12, for example, including, but is not limited to, silicon, silicon on insulator (SOI), stacked SOI (SSOI), stacked SiGe on insulator (S-SiGeOI), SiGeOI, and GeOI, and combinations thereof.

Please replace paragraph 0017 with the following rewritten paragraph:

0017 In an important aspect of the invention, the via openings e.g., 26A and 26B are formed with an aspect ratio[[n]] greater than about 1.5, more preferably greater than about 2.8, preferably having substantially vertical sidewalls, for example

having a sidewall angle with respect to horizontal of greater than about 85 degrees. The dielectric insulating layer 24 is preferably formed of a low-K dielectric having a dielectric constant less than about 3.5, most preferably fluorinated silicate glass (FSG) formed by a conventional HDP-CVD or PECVD process, but which may also be formed of another silicon oxide based material such as BPSG or BPTEOS.

Please replace paragraph 0018 with the following rewritten paragraph:

0018 Referring to Figure 1C, a barrier layer e.g., 28 of Ti/TiN, TiN, Ta, TaN, or combinations thereof, is first formed to line the via openings. Preferably the barrier layer is deposited with a thickness less than about 400 Angstroms to decrease[[s]] a contact electrical resistance of the vias. The barrier layer 28 may be deposited by a conventional PVD process with a collimator, but is more preferably deposited according to a low temperature and low pressure magnetron sputtering process, for example at a temperature less than about 400 °C, including at about room temperature for example, less than about 30 °C, and at a pressure of less than about 5 milliTorr.

Please replace paragraph 0019 with the following rewritten paragraph:

0019 In another aspect of the invention, following formation of the barrier layer 28, preferably according to a magnetron sputtering process the remaining portion of the via openings are filled with an AlCu alloy filling 30, according to a low pressure magnetron sputtering process, preferably at pressures less than about 5 milliTorr, and at temperatures less than about 400 °C, including at about room temperature for example, less than about 30 °C. The AlCu preferably has a copper content of about 2 to about 10 atomic weight percent with respect to aluminum. In the case magnetron sputtering is used to form the barrier layer, the AlCu deposition may be performed in-situ, improving metal adhesion to the barrier layer. Alternatively, the barrier layer 28 may be formed by a conventional PVD process prior to depositing the AlCu by the low temperature/low pressure magnetron sputtering process.

Please replace paragraph 0027 with the following rewritten paragraph:

0027 Referring to Figure 3 is a process flow diagram including several embodiments of the present invention. In a first process 301, a semiconductor substrate including CMOS transistors with salicide[[s]] contact areas is provided. In process 303, a PMD dielectric insulating layer is formed over the CMOS transistors. In process 305, first vias are formed in closed communication with salicide areas. In process 307, a first barrier layer is formed to line the first vias. In process 309, an AlCu layer is deposited by <u>a</u> low temp<u>erature</u> process to backfill the vias according to preferred embodiments including a portion overlying the PMD layer. In process 311, AlCu interconnect lines are patterned and etched in the overlying AlCu portion. In process 313, a second barrier layer is formed over the AlCu interconnect lines. In process 315, an IMD dielectric insulating layer is formed over the interconnect lines. As indicated by process arrow 317, processes 307 through 315 are sequentially repeated to form AlCu vias and interconnect lines in overlying levels through at least the third metallization level (M3).